REMARKS

The Applicants request reconsideration of the rejection.

Claims 1-15 are pending.

Submitted herewith is a certified copy of the corresponding Japanese patent application (JP 2001-038678, filed February 15, 2001). An indication that this document has been safely received would be appreciated.

The title of the invention has been amended as required by the Examiner.

The claims have been amended, without narrowing their scope, to address the Examiner's objections set forth on pages 2-4 of the Office Action. For the Examiner's convenience, "NG" ("no good") has been replaced with --NO--, and "OK" has been replaced with --YES--. The specification has also been amended accordingly. No new matter issues are believed to be raised by substituting one well-known expression for another.

Claims 1-15 were rejected under 35 U.S.C. §112, second paragraph, as set forth on pages 4-5 of the Office Action. The claims have been amended, without narrowing their scope, to address the Examiner's concerns.

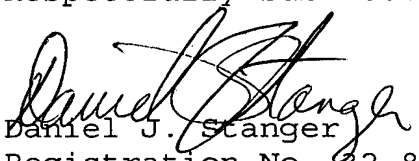
Claims 1-3 and 8 were rejected under 35 U.S.C. §102 as being anticipated by Cheng, et al., U.S. 6,367,060 (Cheng). The Applicants traverse as follows.

The present invention, as defined in claims 1-3 and 8, is directed to a method of designing a semiconductor integrated circuit in which a chip is divided into a number of areas, and a plurality of clock pins are provided for each area. The areas are defined and the clock pins provided in advance of the disposition of logical cells, thereby permitting the circuit to be designed with a minimum of delay fluctuations. In contrast, Cheng groups clock tree nodes sequentially according to the distribution of clock input pins of flip-flops which are to be the final nodes of clock signal feeding, thereby finally assembling the tree to the clock source pins. Thus, Cheng prepares the areas in accordance with an already-established distribution state of the nodes, thereby to generate plural clock pins.

Furthermore, whereas Cheng adjusts clock timing in accordance with node grouping based on buffer type, the present invention establishes and chooses from among a plurality of methods of adjusting clock signal timing. In addition, the invention groups at each clock timing required by each flip-flop, but Cheng groups based on the position of the clock input pins.

In view of the foregoing remarks and amendments, Applicants request reconsideration of the rejection and allowance of the claims.

Respectfully submitted,



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